High Definition Audio SoundMAX Codec

AD1882A

FEATURES

- Six 192 kHz, 95 dB DACs
  - All independent sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit PCM resolution
  - Selectable stereo mixer on outputs
- Four 192 kHz, 90 dB ADCs
  - Simultaneous record of up to 2 stereo channels
  - All independent sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit resolution
- S/PDIF output
  - Supports all sample rates 44.1 kHz through 192 kHz
  - 16-, 20-, and 24-bit data widths; PCM and AC3 formats
  - Digital PCM gain control
- Dedicated auxiliary pins
  - Stereo CD input w/GND sense
  - Mono out pin for internal speaker with EAPD support
  - Analog PCBeep input pin
- Stereo digital microphone
  - Two 192 kHz digital microphone channels
  - Supports 1 or 2 microphones on 1 pin
  - Selectable bit clock rates of 1.5 MHz, 2.0 MHz, and 3.0 MHz
  - All sample rates, 8 kHz through 192 kHz
  - 16-, 20-, and 24-bit resolution
- Microsoft Vista Premium® logo for notebook and desktop
- Impedance and presence detection on all jack pins
- 2 general-purpose digital I/O (GPIO) pins
- Advanced power management modes
- EAPD control for internal speakers
- 3.3 V analog and digital supply voltage
- 1.5 V and 3.3 V HD Audio link signaling
- Very low power consumption in D3 state

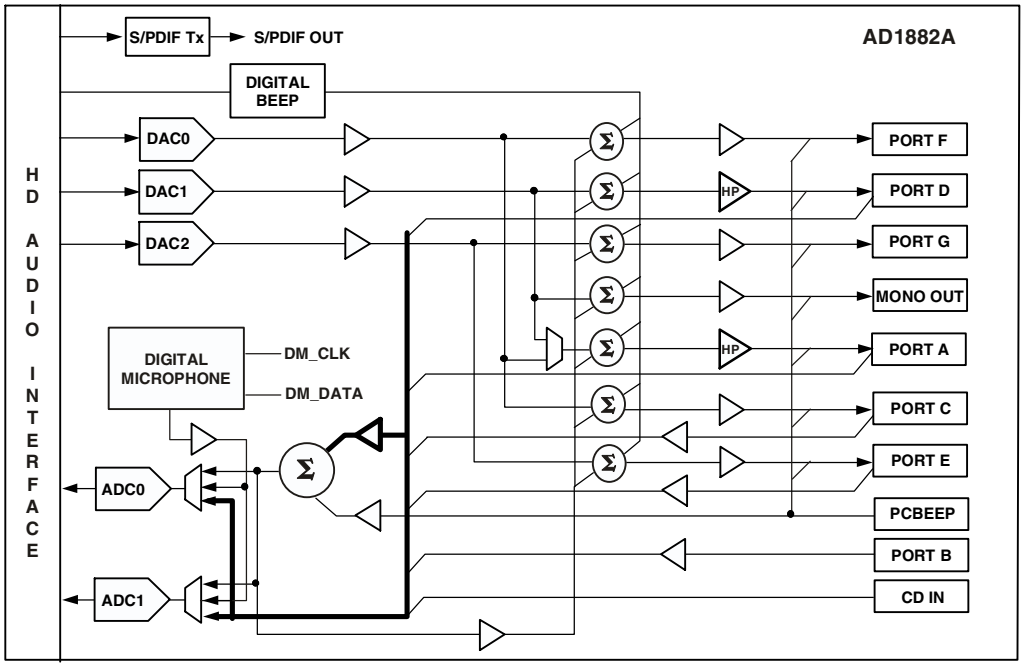

Figure 1. AD1882A Block Diagram

Rev. 0

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REVISION HISTORY

8/08—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD1882A audio codec and SoundMAX® software provides superior HD audio quality that exceeds Vista Premium performance. The AD1882A has six DACs and four ADCs, two stereo headphone ports, C/LFE swapping, digital and analog PCBeep, and S/PDIF output, making the AD1882A the right choice for desktop and notebook PCs where performance is the primary consideration.

The jack retasking feature on this product supports various configurations including platforms for 5.1 on 5 or 3 jacks, and front panel jack retasking.

The AD1882A is available in a 48-lead Pb-free lead frame chip scale package in both reels and trays. See Ordering Guide on Page 17.

SPECIAL SOFTWARE FEATURES

The AD1882A audio codec also supports the following additional software features:

- BlackHawk® and SoundMAX GUI contain all user audio controls
- Voice input enhancements: Andrea Electronics best-in-class noise reduction, beam forming, and echo cancellation
- Output enhancements: Sensaura/Sonic Focus, spreading/downmixing, MP3 refinement, adaptive dynamics, compressor/limiter, speaker/graphic EQ, Voice Clarity/X-Matrix™, AGC, UI tuning tools
- DTS®, SRS®, EAX for gaming

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1882A SoundMAX codec's architecture and functionality. Additional information on the AD1882A is available in the AD1882A Programmers Reference Manual. Please contact your local Analog Devices, Inc., sales representative for more information. For information on SoundMAX codecs and software, see Analog Devices website at http://www.analog.com/soundMAX.

JACK CONFIGURATION

The guidelines shown in Table 1 through Table 4 should be used when selecting ports for particular functions.

Table 1. Typical Desktop Configuration with Discrete Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone
Port F	Rear Panel Surround
Port G	Rear Panel C/LFE

Table 2. Typical Desktop Configuration with 5.1 on 3 Jacks

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Surround
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone/C/LFE

Table 3. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line/Microphone In

Table 4. Typical Notebook Configuration with Digital Microphone

Port	Function
Port A	Headphone
Port B	Microphone
Digital Microphone	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line/Microphone In

SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_S	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	–3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line-Out Tests
	32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 kΩ Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–85		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Headphone Drive (32 Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–83		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Input Ports (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–81		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS—f_S = 8 kHz to 96 kHz[1]				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection				dB
Group Delay		+20	–100	$1/f_S$
Group Delay Variation Over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[2]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line Inputs to Other		–100	–80	dB

Parameter		Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Resolution			24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[1]				±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)				±0.5	dB
DAC Crosstalk					dB
(Input L, Zero R, Read R_OUT; Input R, Zero L, Read L_OUT)[1]			–95		dB
DAC VOLUMES					
Step Size (DAC0, DAC1, DAC2)			1.5		dB
Output Gain/Attenuation Range		–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ADC VOLUMES					
Step Size (ADCSEL-0, ADCSEL-1)			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ANALOG MIXER					
Signal-to-Noise Ratio (SNR) Input to Output			95		dB
Step Size: All Mixer Inputs			1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage		1.0			V rms[3]
Ports C, E, F, and G Mono Out		2.83			V p-p
	Output Impedance[1]			300	Ω
	External Load Impedance[1]	10			kΩ
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage		1.0			V rms[3]
Ports A and D		2.83			V p-p
	Output Impedance[1]			0.5	Ω
	External Load Impedance[1]	32			Ω
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG INPUTS					
CD, Port D (When Used as Input)			1		V rms[3]
			2.83		V p-p
Microphone Boost Amplifier, Ports B, C, or E (When Used as Inputs)	Boost = 0 dB		1		V rms[3]
			2.83		V p-p
	Boost = 10 dB		0.316		V rms[3]
			0.894		V p-p
	Boost = 20 dB		0.1		V rms[3]
			0.283		V p-p
	Boost = 30 dB		0.032		V rms[3]
			0.089		V p-p
Input Impedance[1]			20		kΩ
Input Capacitance[1]			5	7.5	pF
DIGITAL GPIO PINS: GPIO_0, GPIO_1/EAPD					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High), (I_{IH})			150		nA
Input Leakage Current (Signal Low), (I_{IL})			50		µA
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
DM_CLK					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V

Parameter		Min	Typ	Max	Unit
DM_DATA					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		nA
S/PDIF_OUT					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{GPIO} \times 0.10$	V
POWER SUPPLY					
Analog (AV_{DD}) 3.3 V ± 5%					
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			116		mW
Supply Current			35		mA
Digital (DV_{DD}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			162		mW
Supply Current			49		mA
Digital I/O (DV_{IO}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.20		mA
Digital I/O (DV_{IO}) 1.5 V ± 5.5%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.20		mA
Digital GPIO (DV_{GPIO}) 3.3 V ± 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.63		mW
Supply Current			1.10		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)[1]			80		dB

[1] Guaranteed but not tested.
[2] Measurements reflect main ADC.
[3] RMS values assume sine wave input.

HD AUDIO LINK SPECIFICATIONS

HD Audio signals comply with the High Definition Audio specifications. Please refer to these specifications at:
http://www.intel.com/standards/hdaudio/

POWER-DOWN STATES

Table 5. Power-Down States

Parameter	IDV_{DD} Typ	IAV_{DD} Typ	Unit
Function Node In D0, All Nodes Active	49	35	mA
Function Node in D3	16	0.7	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual Block Power Savings			
DAC Pair Powered Down Saves (Each)	6	6	mA
ADC Pair Powered Down Saves (Each)	5	4.4	mA
Mixer Power Control (and Associated Amps) Saves	0	3	mA
MIC_BIAS Powered Down Saves[1]	0	1.0	mA

[1] Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits, setting them to the high-Z state.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Digital GPIO (DV_{GPIO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} + 0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = case temperature in °C
PD = power dissipation in W
θ_{CA} = thermal resistance (case-to-ambient)
θ_{JA} = thermal resistance (junction-to-ambient)
θ_{JC} = thermal resistance (junction-to-case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	47	15	32	°C/W

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

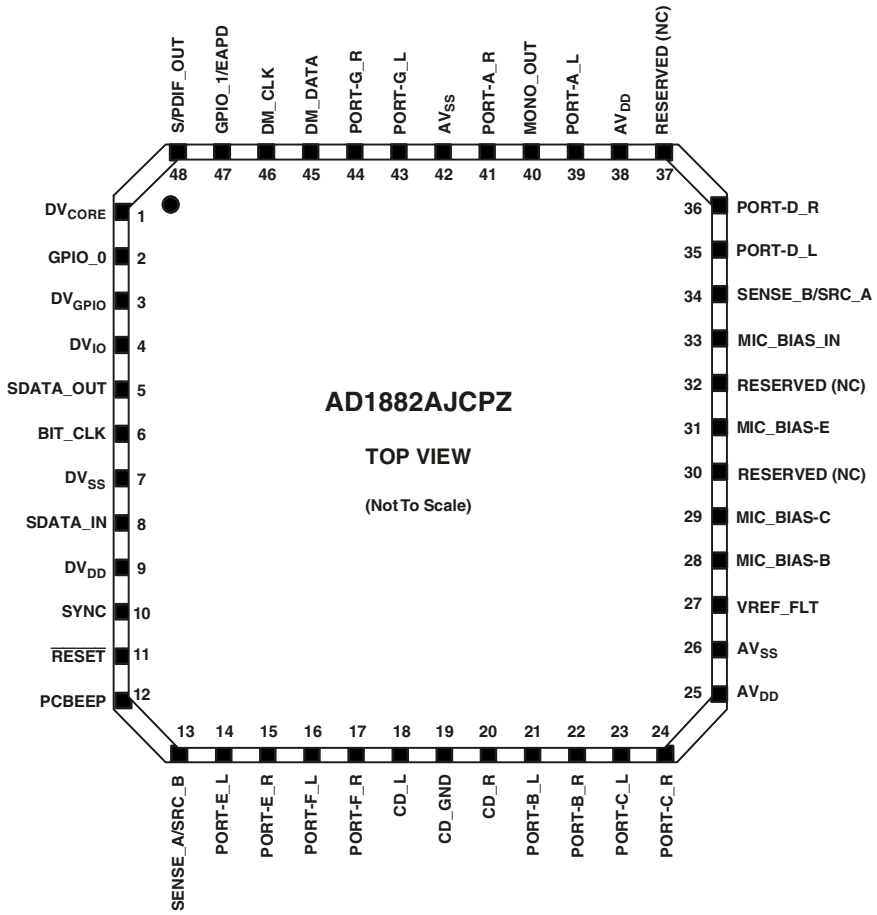

Figure 2. AD1882A 48-Lead Package and Pinout

Table 6. AD1882A Pin Descriptions

Mnemonic	Pin No.	Function	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. AD1882A input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1882A output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. AD1882A master hardware reset
DIGITAL I/O			
GPIO_0	2	I/O	General-Purpose Input/Output. Supports S/PDIF output as primary function.
GPIO_1/EAPD	47	I/O	General-Purpose Input/Output Pin/EAPD Pin. Digital signal used to control external circuitry. By default pin is in a high-Z state. When used as EAPD: high-Z = amp-on, DV_{SS} = amp off.
S/PDIF_OUT	48	O	S/PDIF output.
DM_DATA	45	I	Digital Microphone Data Input. Support for 2 digital microphones
DM_CLK	46	O	Digital Microphone Clock Output.
JACK SENSE AND EAPD			
SENSE_A/SRC_B	13	I/O	JACK SENSE A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	I/O	JACK SENSE E-H Input/Sense A Drive.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	I/O	Auxiliary Input/Output Left Channel.
PORT-F_R	17	I/O	Auxiliary Input/Output Right Channel.
CD_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD Audio Analog Ground Reference (for Differential CD Input). Must be connected to AGND via 0.1 µF capacitor if not in use as CD_GND.
CD_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
FILTER/REFERENCE			
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
DV_{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 µF, 1.0 µF, and 0.1 µF connected in parallel between Pin 1 and DV_{SS} (Pin 4).
VREF_FLT	27	O	Voltage Reference Filter. This pin must be connected to filter caps: 1.0 µF and 0.1µF connected in parallel between Pin 27 and AV_{SS} (Pins 26, 42).

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier, SWAP = outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

Table 6. AD1882A Pin Descriptions (Continued)

Mnemonic	Pin No.	Function	Description
POWER AND GROUND			
DV_{IO} 3.3 V ± 10% or DV_{IO} 1.5 V ± 5.5%	4	I	Connect to the I/O Voltage Used for the HD Audio Controller Signals.
DV_{GPIO}	3	I	Connect to 3.3 V digital supply to power the GPIO and S/PDIF pins.
DV_{SS}	7	I	Digital Supply Return (Ground).
DV_{DD} (3.3 V)	9	I	Digital Supply Voltage 3.3 V. This is regulated down to DV_{CORE} on Pin 1 to supply the internal digital core internal to the AD1882A.
AV_{DD} (3.3 V)	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog Supply Voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source Power for Microphone Bias Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way, the AD1882A is capable of providing 3.9 V as a mic bias to all of the MIC_BIAS pins. If 5 V is not available, connect this pin to 3.3 V (AV_{DD}) via a low-pass filter.
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1882A.

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier, SWAP = outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).

DIGITAL MICROPHONE INTERFACE TIMING SPECIFICATIONS

The digital microphone interface can support one or two digital microphones using two or three codec pins. Both uniplex (one microphone per data pin) and multiplex (two microphones sharing the same data pin) are supported. The timing for these configurations are shown in Figure 3 and Figure 4. The interface can generate a microphone clock at 1.5 MHz, 2.0 MHz, or 3.0 MHz to suit quality and power requirements.

Table 7. Microphone Timing Parameters

Parameter		Min	Typ	Max	Unit
Timing Requirements					
t_0	DM_CLK (1.5 MHz) Period		667		ns
	Duty Cycle		50/50		%
t_0	DM_CLK (2.0 MHz) Period		500		ns
	Duty Cycle		50/50		%
t_0	DM_CLK (3.0 MHz) Period		333		ns
	Duty Cycle		50/50		%
t_1	DM_CLK Rise Time			5	ns
t_2	DM_CLK Fall Time			5	ns
t_3	Data Setup to DM_CLK Edge	100			ns
t_4	Data Hold from DM_CLK Edge	5			ns

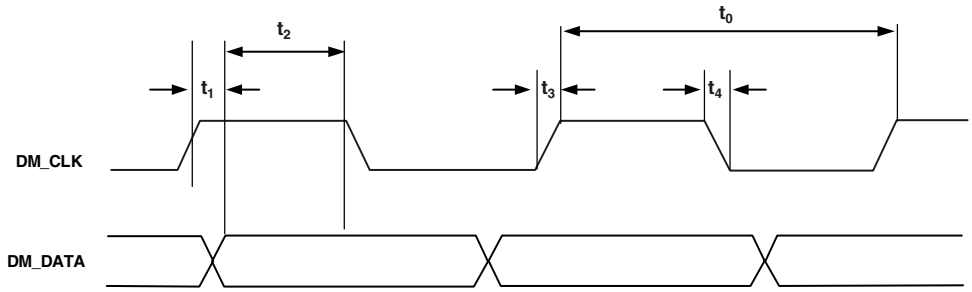

Figure 3. Uniplex Microphone Timing

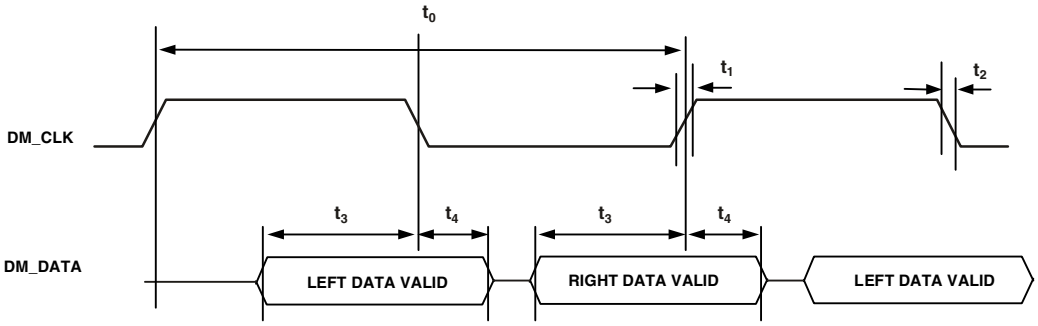

Figure 4. Multiplex Microphone Timing

HD AUDIO PARAMETERS

The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 8. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02[1]	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D4882A		00100100		00010001			
01	FUNCTION					0002003B	00000001	00010C0C	40000002

[1] Subject to change with silicon stepping.

Table 9. SubSystem ID [1]

Node ID	Name	Value	31:16 SSID	15:8 SKU	7:0 Asm ID
01	FUNCTION	BFD20000	BFD2	00	00

[1] The default SSID is overwritten by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.

WIDGET PARAMETERS

Table 10. Widget Parameters

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	ConnList Length 0E	Power States 0F	Output Amp Capabilities 12
01	0x0000 0480	0x000E 07FF	0x0000 0001		0x80000000		0x0000 0009	0x0005 2727
02	0x0003 031D	0x000E 07E0	0x0000 0005			0x0000 0001		0x8005 2727
03	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
04	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
05	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
08	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
09	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
0C	0x0030 010D					0x0000 0008		0x8005 3627
0D	0x0030 010D					0x0000 0008		0x8005 3627
10	0x0070 000C					0x0000 0000		0x800B 0F0F
11	0x0040 058D			0x0000 373F		0x0000 0001		0x8000 0000
12	0x0040 058D			0x0001 003F		0x0000 0001	0x0000 0009	0x8000 0000
13	0x0040 050C			0x0001 0010		0x0000 0001	0x0000 0009	0x8005 1F1F
14	0x0040 0081			0x0000 3727		0x0000 0000		
15	0x0040 018D			0x0000 3737		0x0000 0001		0x8000 0000
16	0x0040 058D			0x0001 0017		0x0000 0001	0x0000 0009	0x8000 0000
17	0x0040 098D			0x0000 3737		0x0000 0001		0x8000 0000
18	0x0040 0081			0x0000 0024		0x0000 0000		
19	0x0050 0500					0x0000 0002	0x0000 0009	
1A	0x0040 0000			0x0000 0020		0x0000 0000		
1B	0x0040 0301			0x0000 0010		0x0000 0001		
1E	0x0020 0103				0x8000 0000	0x0000 0002		
1F	0x0040 000B			0x0000 0020	0x0017 0300	0x0000 0000		
20	0x0020 010B				0x8005 1F17	0x0000 0008		
21	0x0030 010D					0x0000 0001		0x8005 1F1F
22	0x0020 0103				0x8000 0000	0x0000 0002		
23	0x00F0 0100					0x0000 0008		
24	0x0040 098D			0x0000 0017		0x0000 0001		0x8000 0000
26	0x0020 0103				0x8000 0000	0x0000 0002		
27	0x0020 0103				0x8000 0000	0x0000 0002		
29	0x0020 0103				0x8000 0000	0x0000 0002		
2A	0x0020 0103				0x8000 0000	0x0000 0002		
2C	0x0020 0103				0x8000 0000	0x0000 0002		
2D	0x0020 0100					0x0000 0001		
2F	0x00F0 0100					0x0000 0003		
37	0x0030 0101					0x0000 0002		
39	0x0030 010D					0x0000 0001		0x0027 0300
3A	0x0030 010D					0x0000 0001		0x0027 0300
3C	0x0030 010D					0x0000 0001		0x0027 0300

HD AUDIO WIDGETS

In the following table, node IDs that are not shown are reserved for future use.

Table 11. HD Audio Widgets

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device Identification
01	FUNCTION	x	Function	Designates this Device as an Audio Codec
02	S/PDIF DAC	0	Audio Output	S/PDIF Digital Stream Output Interface
03	DAC_0	0	Audio Output	Headphone/Surround Side (7.1) Channel Digital/Audio Converters
04	DAC_1	0	Audio Output	Stereo Front Channel Digital/Audio Converters
05	DAC_2	0	Audio Output	Stereo C/LFE Channel Digital/Audio Converters
08	ADC_0	1	Audio Input	Stereo Record Channel 1 Audio/Digital Converters
09	ADC_1	1	Audio Input	Stereo Record Channel 2 Audio/Digital Converters
0C	ADC Selector 0	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC0
0D	ADC Selector 1	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC1
10	Digital Beep	7	Beep Generator	Internal Digital PCBeep Signal
11	Port A (Headphone)	4	Pin Complex	Front Panel Headphone/Microphone Jack
12	Port D (Front L/R)	4	Pin Complex	Rear Panel Front/Headphone Jack
13	Mono Out	4	Pin Complex	Monorail Output Pin (Internal Speakers or Telephony System)
14	Port B (Front Mic)	4	Pin Complex	Front Panel Microphone/Headphone Jack
15	Port C (Line In)	4	Pin Complex	Rear Panel Line-In Jack
16	Port F (Surr Back)	4	Pin Complex	Rear Panel Surround-Rear (5.1) Jack
17	Port E (Rear Mic)	4	Pin Complex	Rear Panel Mic Jack
18	CD In	4	Pin Complex	Analog CD Input
19	Mixer Power Down	5	Power Widget	Powers Down the Analog Mixer and Associated Amps
1A	Analog PCBeep	4	Pin Complex	External Analog PCBeep Signal Input
1B	S/PDIF Out	4	Pin Complex	S/PDIF Output Pin
1E	Mono Out Mixer	2	Audio Mixer	Selects Which Source Drives the Mono Out Signal
1F	Digital Microphone	4	Pin Complex	Digital Microphone Interface
20	Analog Mixer	2	Audio Mixer	Mixes Individually Gainable Analog Inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the Mixer Output to Drive the Port Mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and Mixer Output Amps to Drive Port A
23	VREF Power Down	F	Vendor Defined	Powers Down the Internal and External VREF Circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear Panel C/LFE Jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC1 and Mixer Output Amps to Drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC1 and Mixer Output Amps to Drive Port G
29	Port D Mixer	2	Audio Mixer	Mixes DAC0 and Mixer Output Amps to Drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC2 and Mixer Output Amps to Drive Port F
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C Selected DAC and Mixer Output Amps to Drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the Stereo L/R Channels to Drive Mono Output
2F	BIAS Power Down	F	Vendor Defined	Powers Down the Internal MIC_BIAS_IN and all MIC_BIAS Pins
37	Port A Out Selector	3	Audio Selector	Selects the Port A DAC (0, 1)
39	Port B Boost	3	Audio Selector	Microphone Boost Amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone Boost Amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone Boost Amp for Port E

CONNECTION LIST

Table 12. Connection List

	Connections		0	1		2		3		4		5		6		7	
Node ID	**[0–3]**	**[4–7]**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**	**I**	**NID**
02	0x0000 001D		1D														
03																	
04																	
05																	
08	0x0000 000C		0x0C														
09	0x0000 000D		0x0D														
0C	0x18BC 3911	0x2012 3B1F	0x11		0x39	1	0x3C		0x18		0x1F		0x3B		0x12		0x20
0D	0x18BC 3911	0x2012 3B1F	0x11		0x39	1	0x3C		0x18		0x1F		0x3B		10x2		0x20
10																	
11	0x0000 0022		0x22														
12	0x0000 0029		0x29														
13	0x0000 002D		0x2D														
14																	
15	0x0000 002C		0x2C														
16	0x0000 002A		0x2A														
17	0x0000 0026		0x26														
18																	
19	0x0000 2120		0x20		0x21												
1A																	
1B	0x0000 0002		0x02														
1E	0x0000 2104		0x04		0x21												
1F																	
20	0x1211 3A39	0x1A18 3B3C	0x39		0x3A		0x11		0x12		0x3C		0x3B		0x18		0x1A
21	0x0000 0020		0x20														
22	0x0000 2137		0x37		0x21												
23	0xA220 9811	0xBC30 AE24	0x11	1	0x18		0x20	1	0x22		0x24	1	0x2E		0x30	1	0x3C
24	0x0000 0027		0x27														
26	0x0000 2105		0x05		0x21												
27	0x0000 2105		0x05		0x21												
29	0x0000 2104		0x04		0x21												
2A	0x0000 2103		0x03		0x21												
2C	0x0000 2103		0x03		0x21												
2D	0x0000 001E		0x1E														
2F	0x0017 1514		0x14		0x15		0x17										
37	0x0000 0403		0x03		0x04												
39	0x0000 0014		0x14														
3A	0x0000 0015		0x15														
3C	0x0000 0017		0x17														

DEFAULT CONFIGURATION BYTES

In Table 13, default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

Table 13. Default Configuration Bytes

		31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
			Location					Misc.		
Name	Value	Connectivity	Chassis	Position	Def. Device	Conn Type	Color	JD	Def Assn	Sequence
Port A (Headphone)	0x0221 401F	Jack	External	Front	HP Out	1/8" Jack	Green	0	1	F
Port D (Front L/R)	0x0101 4010	Jack	External	Rear	Line Out	1/8" Jack	Green	0	1	0
Mono Out	0x9017 01F0	Fixed	Internal	N/A	Speaker	Other Analog	Unknown	1	F	0
Port B (Front Mic)	0x02A1 90F0	Jack	External	Front	Mic In	1/8" Jack	Pink	0	F	0
Port C (Line In)	0x0181 3021	Jack	External	Rear	Line In	1/8" Jack	Blue	0	2	1
Port F (Surr Back)	0x0101 1012	Jack	External	Rear	Line Out	1/8" Jack	Black	0	1	2
Port E (Rear Mic)	0x01A1 9020	Jack	External	Rear	Mic In	1/8" Jack	Pink	0	2	0
CD IN	0x9933 012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	0x90F7 01F0	Fixed	Internal	N/A	Other	Other Analog	Unknown	1	F	0
S/PDIF Out	0x0145 11F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
Digital Microphone	0x97A6 09F0	Fixed	Internal	Special 1	Mic In	Other Digital	Unknown	1	F	0
Port G (C/LFE)	0x0101 6011	Jack	External	Rear	Line Out	1/8" Jack	Orange	0	1	1

OUTLINE DIMENSIONS

Dimensions are shown in millimeters.

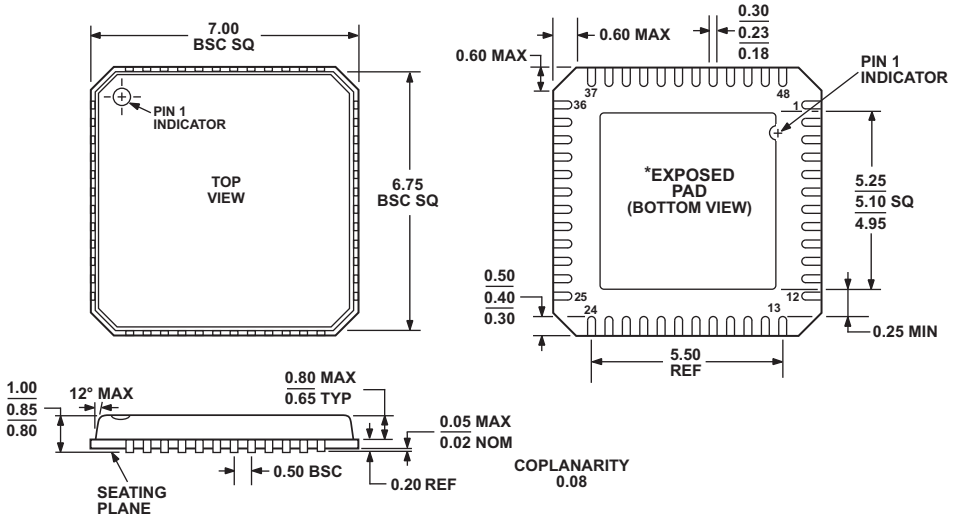

Figure 5. 48-Lead, Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm x 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1882AJCPZ[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1882AJCPZ-RL[1]	0°C to 70°C	48-Lead LFCSP_VQ, 13" Tape and Reel	CP-48-1

[1] Z = RoHS Compliant Part.

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